REMARKS

Claims 1-2 and 4 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Harkin et al. (U.S. Patent no. 5,999,200; hereinafter Harkin) in view of White , et al. (U.S. Patent no. 5,918,225; hereinafter White).

White is a SQL-Based database and teaches nothing about enhancing the rendering of pixels in the case of opcoder with a core loop that has above and below the normal table area boundary checks for the index to avoid accessing outside the lookup table area that introduce the additional instructions and time. There is no teaching or suggestion of such a core loop in the opcode in White that so there is no teaching to remove it. The examiner is combining references that are unrelated and where there is no suggestion in the references to such a combination. The problem and solution is neither taught nor suggested in these references. As taught in applicant's specification applicant's core loop of the opcode should have two boundary checks for the index to avoid accessing outside the lookup table area. These checks introduce the additional instructions and time for which applicant is trying save buy the present invention. The applicant's solution for this is by applicant's claim 1 that calls for" determining maximum and minimum values of index of normal table area of a lookup table, and expanding the lookup table opcodes above and below said maximum and minimum values of said index and removing core loop checks."

As stated in the specification the prior implementation required about 4-5 clocks for each pixel. The total rendering clock count is reduced to two clock steps by the

improved claimed steps. This is not taught in these references. The examiner acknowledges that Harkin does not disclose the step of determining the maximum and minimum values of index, and expanding the look up table opcodes. The examiner states that White discloses (column 51, lines 39-57, particularly lines 51-52) the expansion of a lookup table beyond its original range (originally determined to be from 0-255, and then expanded to 0-65535) and the omission of core loop checks (column 51, lines 52-57, by the referenced statement that "there is in fact no special processing required for expanding the value lookup table." The examiner goes on to argue that the expansion of the Harkin lookup table in this manner to accommodate values above the lookup table range (or in a corresponding manner to accommodate values below the lookup table range) would be expedient obvious to one of ordinary skill in the art.

The examiner's argument "or in a corresponding manner to accommodate values below the lookup table range" is not based on anything taught in the White or other references. The examiner has no support for this argument. As stated in the background the core loop of the opcode should have two boundary checks for the index to avoid accessing outside the lookup table area. There is no such opcode in White or two boundary checks. It is a much different problem from that of the White reference to expand a table in both directions than to have an expansion in only one positive direction. There is no need to know the minimum range when you already know the minimum is always zero and you know it only goes one way but this is not so in the present case where as applicant teaches the range goes into negative numbers. Applicant's have examined the White reference and have determined the reference teaches nothing about determining maximum and minimum index values of the table or step 27 in applicant's

Fig. 2 or removing the core loop checks. The White reference simply increases the number of entries from 256 to 65535. It does not teach determining maximum and minimum index values of the table or expanding the lookup table opcodes above and below the minimum values of the index of normal table area.

The statement "there is in fact no special processing required for expanding the value lookup table" is because the values are being assigned to the table as they are arrived. There is nothing in this statement that suggests removing core loop boundary checks. To the contrary, the following sentence on column 51states that the system simply makes sure that it has sufficient space for accommodating the arrival of additional entries. This does suggest some form of boundary check to determine if there is sufficient space. For these reasons it is not seen where applicant's claimed invention would be obvious in view of these references.

Claim 2 further calls for "the expanding step includes the step of replicating the highest value if the index is above the normal table area." This is not taught or suggested in the references and there is nothing that suggests that the highest value be replicated or that it is inherent that the highest value be replicated absent applicant's teaching. To the contrary the White reference expands the indexes form 255 to 65535 and there is no mention of replication.

Claim 4 calls for "the expanding step includes the step of replicating the lowest value if the index is below the normal table area." This is not taught or suggested in the references and there is nothing that suggests that the lowest value be replicated or that it is inherent that the lowest value be replicated absent applicant's teaching. To the contrary the White reference only expands the indexes form 255 to 65535 and there is no mention

of replication or what to do with index values below the normal table area or the reason for doing the steps claimed to save clock counts as discussed previously.

Claim 3 dependent on claim 1 is deemed allowable for at least the same reasons as Claim 1. Claim 3 further calls for said opcodes are for shading. " The examiner references Steiner but Steiner does not teach what is missing in Claim 1.

Claim 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harkin in view of White as applied to claim 1 above and further in view of Lung et al (U.S. Patent No. 5,533,174; hereinafter Lung).

Lung describes a low cost page printer. As admitted by the examiner Lung does not disclose means for rendering to include a lookup table that includes opcode values over all of indexes wherein the index into the lookup table is calculated for every pixel using a base value and a gradient in both x and y directions. The examiner references Harkin to teach this but this is not taught in Harkin for the reasons discussed above.

Applicant's claim 5 calls for "A printer comprising:

a printing device;

a printer controller for controlling said printing device, said printer controller including means for interpreting responsive to each line of source language to translate into machine language and then execute and wherein a figure to be printed is divided into graphics rendering primitives and means for rendering where each and every pixel in the primitive is a function of its position in the primitive, said means for rendering includes a lookup table that includes opcode values over all values of indexes wherein the index into the lookup table is calculated for every pixel using a base value and a gradient in both x and y

directions and said means for providing opcode values for all values of indexes includes an opcoder with a core loop that has above and below the normal table area boundary checks for the index to avoid accessing outside the lookup table area and means for determining maximum and minimum values of index of normal table area of a lookup table, and expanding the lookup table above and below said maximum and minimum values of said index by replicating the highest value if the index is above the normal table value and replicating the lowest value if the index is below the normal table area and removing core loop checks."

As discussed previously this is neither taught nor suggested in the Harkin or White references and is not taught in Lung. There is no provision for providing for all values of indexes, there is no teaching of determining maximum and minimum values of the index and no teaching of replicating the highest value if the index is above the maximum value and replicating the lowest value if the index is below the minimum value. There is no removing of the core loop checks. As stated in the background of the patent application the prior art had delays in the time for rendering pixels occur because of the time taken to access outside the lookup table area. The present application reduces these delays by the determining maximum and minimum values of index of normal table area of a lookup table, and expanding the lookup table above and below said maximum and minimum values of said index by replicating the highest value if the index is above the normal table value and replicating the lowest value if the index is below the normal table area and removing core loop checks. Claim 5 is therefore deemed allowable over these references.

Claim 6 calls for: "a rendering subsystem including a means for generating an index for each pixel in each of said pixels, said rendering subsystem including means for determining maximum and minimum values of index of normal table area of a lookup table and rendering an expanded lookup table for the entire range of index values and removing core loop checks, said rendering lookup table of said rendering subsystem has its highest and lowest values replicated above and below the normal table indexes so as to provide lookup table values for the entire range of indexes."

As discussed previously this is not taught or suggested in the references.

In the examiner's response to arguments the examiner argues that the determining of maximum and minimum index values, the definition of an 8-bit index (White column 51, lines 39-57) inherently determines a minimum of zero and a maximum of 255. This only points out the why White does not apply. There is no core loop of opcodes in White and expansion is always in the positive direction. It is the core loop of the opcode that has the two boundary checks that introduces the additional instructions that increases the time taken and applicant teaches how to overcome that problem and to remove the core loop checks. Neither the problem nor the solution is taught in White or the other references. Further, there is no need to determine a minimum value when expansion is always in one direction above zero. The examiner makes reference to "special processing" but that has nothing to do with core loop checks.

Since there is no other reason for rejection applicant's Claims 1-6 are deemed allowable and an early notice of allowance is deemed in order and is respectfully requested.

Respectfully requested;

Robert L. Troike

Robert L. Troike (Reg. 24183)

Telephone No. (301) 751-0825